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Vishay Siliconix

Automotive N-Channel 100 V (D-S) 175 °C MOSFET



PRODUCT SUMMARY			
V _{DS} (V)	100		
$R_{DS(on)}(\Omega)$ at $V_{GS} = 10 \text{ V}$	0.0920		
$R_{DS(on)}(\Omega)$ at $V_{GS} = 4.5 \text{ V}$	0.1170		
I _D (A) per leg	14		
Configuration	Single		
Package	PowerPAK SO-8L		

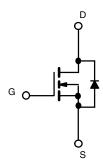
FEATURES

- TrenchFET® power MOSFET
- AEC-Q101 qualified
- 100 % Rq and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912





ROHS COMPLIANT HALOGEN FREE



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise noted)						
PARAMETER		SYMBOL	LIMIT	UNIT		
Drain-source voltage		V _{DS}	100	V		
Gate-source voltage		V _{GS}	± 20	V		
Continuous drain current	T _C = 25 °C	- I _D	14			
	T _C = 125 °C		8			
Continuous source current (diode conduction) ^a		I _S	15	Α		
Pulsed drain current ^b		I _{DM}	17			
Single pulse avalanche current	L = 0.1 mH	I _{AS}	9			
Single pulse avalanche energy	L = 0.111111	E _{AS}	4	mJ		
Maximum power dissipation ^b	T _C = 25 °C	P _D	45	W		
	T _C = 125 °C		15	VV		
Operating junction and storage temperature range		T _J , T _{stg}	-55 to +175	°C		
Soldering recommendations (peak temperature) d, e			260	C		

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	LIMIT	UNIT	
Junction-to-ambient	PCB mount c	R_{thJA}	70	°C/W	
Junction-to-case (drain)			3.3	C/VV	

Notes

- a. Package limited
- b. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %
- c. When mounted on 1" square PCB (FR4 material)
- d. See solder profile (www.vishay.com/doc?73257). The PowerPAK SO-8L is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components



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SPECIFICATIONS (T _C = 25 °C, u	nless otherv	vise noted)					
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		100	-	-	V
Gate-source threshold voltage	$V_{GS(th)}$	V _{DS} =	V_{GS} , $I_D = 250 \mu A$	1.5	2.0	2.5	\ \ \
Gate-source leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$		-	-	± 100	nA
Zero gate voltage drain current	I _{DSS}	$V_{GS} = 0 V$	V _{DS} = 100 V	-	-	1	μA
		$V_{GS} = 0 V$	V _{DS} = 100 V, T _J = 125 °C	ı	-	50	
		V _{GS} = 0 V	V _{DS} = 100 V, T _J = 175 °C	-	-	150	
On-state drain current ^a	I _{D(on)}	V _{GS} = 10 V	$V_{DS} \ge 5 V$	6	-	-	Α
		V _{GS} = 10 V	I _D = 4 A	-	0.0765	0.0920	
Drain actures on atota registance 8	D	V _{GS} = 4.5 V	I _D = 3 A	-	0.0967	0.1170	0
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = 10 V	I _D = 4 A, T _J = 125 °C	-	-	0.1620	Ω
		V _{GS} = 10 V	I _D = 4 A, T _J = 175 °C	-	-	0.2056	
Forward transconductance b	9 _{fs}	V_{DS}	= 15 V, I _D = 4 A	-	8.6	-	S
Dynamic ^b					•		
Input capacitance	C _{iss}		V _{DS} = 25 V, f = 1 MHz	-	212	280	pF
Output capacitance	C _{oss}	$V_{GS} = 0 V$		-	118	160	
Reverse transfer capacitance	C _{rss}			-	15	20	
Total gate charge ^c	Qg		V _{DS} = 50 V, I _D = 3 A	-	4.7	8	nC
Gate-source charge ^c	Q_{gs}	V _{GS} = 10 V		-	0.8	-	
Gate-drain charge ^c	Q _{gd}				1.3	-	
Gate resistance	Rg	f = 1 MHz		2	4	6	Ω
Turn-on delay time °	t _{d(on)}	V_{DD} = 50 V, R_L = 33.3 Ω $I_D \cong$ 1.5 A, V_{GEN} = 10 V, R_g = 1 Ω		-	9	15	
Rise time ^c	t _r			-	5	10	ns ns
Turn-off delay time ^c	t _{d(off)}			-	15	30	
Fall time ^c	t _f			-	5	10	
Source-Drain Diode Ratings and Charact	teristics ^b				•		
Pulsed current ^a	I _{SM}			-	-	17	Α
Forward voltage	V_{SD}	I _F = 4 A, V _{GS} = 0 V		-	0.88	1.2	V
Body diode reverse recovery time	t _{rr}	I _F = 3 A, di/dt = 100 A/μs		-	29	60	ns
Body diode reverse recovery charge	Qrr			-	27	55	nC
Reverse recovery fall time	ta			-	19	-	ns
Reverse recovery rise time	t _b			-	10	-	ns
Body diode peak reverse recovery current	I _{RM(REC)}			1	-1.9	-	Α

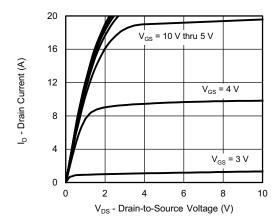
Notes

- a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %
- b. Guaranteed by design, not subject to production testing
- c. Independent of operating temperature

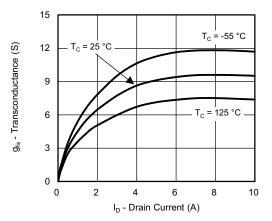
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



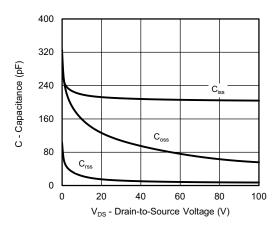
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



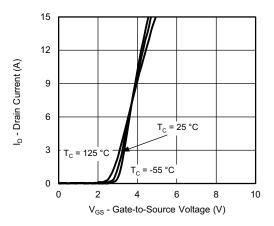
Output Characteristics



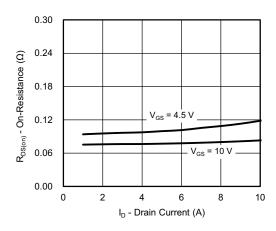
Transconductance



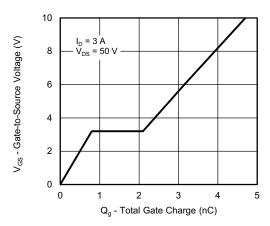
Capacitance



Transfer Characteristics



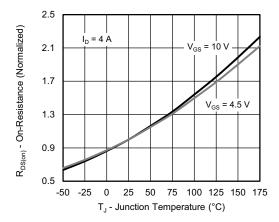
On-Resistance vs. Drain Current



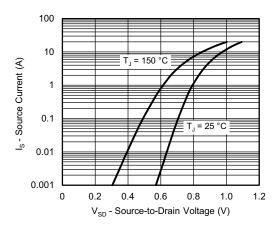
Gate Charge



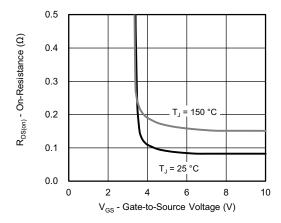
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



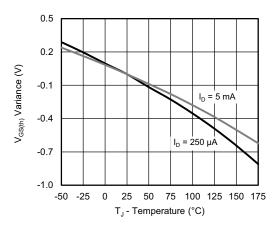
On-Resistance vs. Junction Temperature



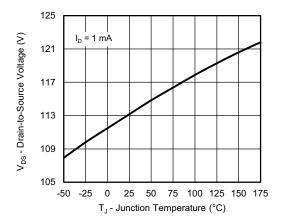
Source Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage



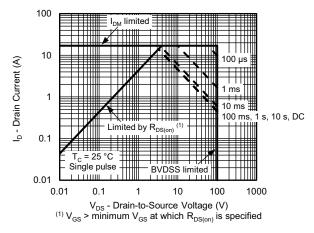
Threshold Voltage



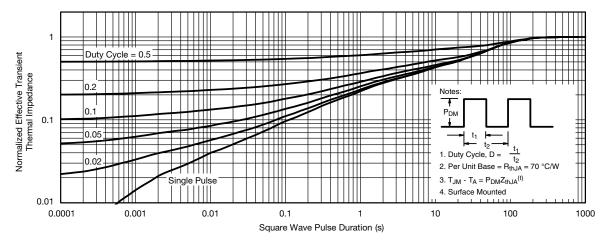
Drain Source Breakdown vs. Junction Temperature



THERMAL RATINGS ($T_A = 25$ °C, unless otherwise noted)



Safe Operating Area

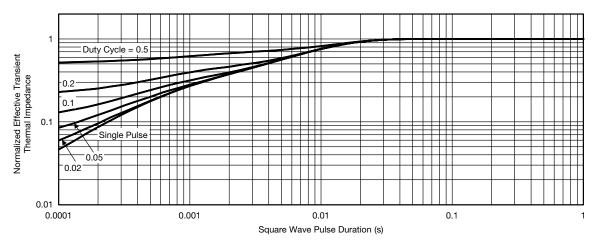


Normalized Thermal Transient Impedance, Junction-to-Ambient

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THERMAL RATINGS (T_A = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case

Note

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
 - Normalized Transient Thermal Impedance Junction-to-Case (25 °C) are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg275561.



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