



General Description

The AOZ1605 is a high-performance, easy-to-use Buck regulator. The 3 MHz switching frequency, low quiescent current and small package size make it an ideal choice for portable applications. The AOZ1605 has a patented light load mode architecture allowing up to 85% efficiency at 1 mA load currents, enabling longer standby times in battery operated systems.

The AOZ1605 operates from a 2.5 V to 5.5 V input voltage range and provides up to 500 mA of output current with an output voltage adjustable down to 0.6 V.

The AOZ1605 is available in a tiny 2 mm x 2 mm 8-pin DFN package and is rated over a -40 °C to +85 °C ambient temperature range.

Features

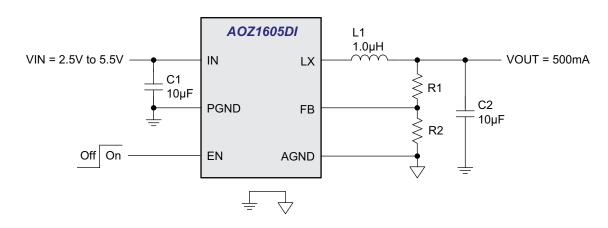
- 2.5 V to 5.5 V input voltage range
- 30 μA quiescent current
- 0.05 μA shutdown current
- Output voltage adjustable to 0.6 V
- Fixed output voltages available
- ± 1.5% initial accuracy
- Up to 500 mA continuous output current
- 3 MHz constant frequency operation
- Low drop-out operation: 100% duty cycle
- Cycle-by-cycle current-limit
- Thermal overload protection
- Excellent load transient response
- Internal soft-start
- Tiny 2 mm x 2 mm DFN-8 package

Applications

- Smart phones
- Personal media players
- MP3 players
- Digital still cameras
- Wireless modems and LANs
- Portable USB devices



Typical Application





Ordering Information

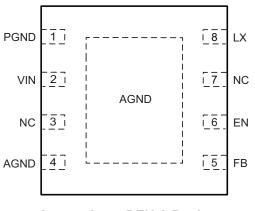
Part Number	Output Voltage	Marking	Temperature Range	Package	Environmental
AOZ1605DI	Adjustable	0	-40 °C to +85 °C	2 x 2 DFN-8	Green Product



AOS Green Products use reduced levels of Halogens, and are also RoHS compliant.

Please visit www.aosmd.com/media/AOSGreenPolicy.pdf for additional information.

Pin Configuration



2mm x 2mm DFN-8 Package (Top View)

Pin Description

Pin Number	Pin Name	Pin Function
1	PGND	Power Ground
2	VIN	Input Supply Pin
3, 7	NC	No Connect Pin
4	AGND	Analog Ground
5	FB	Feedback Input. Connect an external resistive voltage divider to FB to set the output voltage.
6	EN	Enable Input. The device is enabled when EN is high and disabled when EN is low.
8	LX	Switching Node
Pad	AGND	Analog Ground



Absolute Maximum Ratings

Exceeding the Absolute Maximum Ratings may damage the device.

Parameter	Rating
IN, EN, FB to AGND	-0.3 V to +6 V
LX to AGND	-0.3 V to V _{IN} + 0.3 V
PGND to AGND	-0.3 V to +0.3 V
Junction Temperature (T _J)	+150 °C
Storage Temperature (T _S)	-65 °C to +150 °C
Maximum Soldering Temperature (10s)	+300 °C
ESD Rating ⁽¹⁾	2 kV

Note:

1. Devices are inherently ESD sensitive, handling precautions are required. Human body model rating: $1.5k\Omega$ in series with 100pF.

Recommended Operating Conditions

The device is not guaranteed to operate beyond the Maximum Recommended Operating Conditions.

Parameter	Rating
Supply Voltage (V _{IN})	2.5 V to 5.5 V
Ambient Temperature (T _A)	-40 °C to +85 °C
Junction Temperature (T _J)	Internally Limited
Package Thermal Resistance	
2 x 2 DFN-6 (Θ_{JA})	55 °C/W

Electrical Characteristics

 $T_A = 25$ °C, $V_{IN} = 3.6$ V, EN = IN, unless otherwise specified. Specifications in **BOLD** indicate a temperature range of -40 °C to +85 °C.

Symbol	Parameter	Conditions	Min.	Тур.	Max	Units
V _{IN}	Input Voltage Range		2.5		5.5	V
V _{UV}	Under-Voltage Lockout		2.11	2.3	2.49	V
	Under-Voltage Lockout Hysteresis			100		mV
I _{IN}	Input Supply Current	EN = IN, V _{FB} = 1 V, no load		30	55	μΑ
		EN = AGND		0.05	0.1	
V _{FB}	Feedback Reference Voltage	T _A = +25 °C, no load	0.588	0.600	0.612	V
		T _A = -40 °C to +85 °C, no load	0.585	0.600	0.615	
	Feedback Line Regulation	V _{IN} = 2.5 V to 5.5 V		0.3		% / V
	Feedback Load Regulation	0 to 500 mA load		-0.001		% / mA
I _{FB}	Feedback Bias Current			0.01	0.1	μΑ
	Enable Input High Voltage		1.2			V
	Enable Input Low Voltage				0.4	V
I _{EN}	Enable Bias current	V _{EN} = 5.5 V		0.01	0.1	μΑ
OSCILLAT	OR					
f _{SW}	Switching Frequency		2.25	3	3.75	MHz
D _{MAX}	Maximum Duty Cycle		100			%
T _{(ON)MIN}	Minimum On-Time			60		ns
PROTECT	ION					
I _{LIM+}	Positive Current Limit		0.7	1.2		Α
	Thermal Shutdown Threshold			+145		°C
	Thermal Shutdown Hysteresis			40		°C
OUTPUT S	TAGE					
R _{DS(ON)P}	PFET On Resistance	I _{LX} = 50 mA sourcing		400		mΩ
R _{DS(ON)N}	NFET On Resistance	I _{LX} = 50 mA sinking		250		mΩ
	LX Leakage Current	V_{EN} = 0 V, V_{LX} = 0 V or V_{IN} , V_{IN} = 5 V			1	μA
	Efficiency	V _{IN} = 3.6 V, V _{OUT} = 1.8 V, 200 mA load		90		%



Output Voltage Selection for AOZ1605

The output voltage of the AOZ1605 ca be programmed through the resistor network connected from Vout to Feedback to Analog Ground. The resistor from FB to Analog Ground should be 100 k Ω to keep the current drawn through this network below the 6 μ A quiencent current level in PFM mode. The output voltage of the adjustable AOZ1605 parts ranges from 0.6 V to 3.3 V. The output voltage formula is:

$$V_{OUT} = V_{FB} \left(\frac{R1}{R2} + 1 \right)$$

where;

 V_{OUT} = Output Voltage (V)

V_{FB} = Feedback Voltage (0.6 V typical)

R1 = Feedback Resistor from Vout to FB (Ω)

R2 = Feedback Resistor from FB to AGND (Ω)

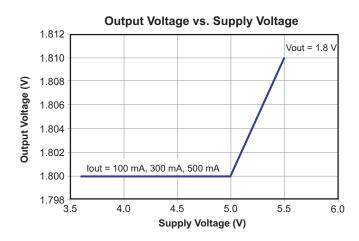
A 100 pF bypass capacitor C5 on the evaluation board, in parallel with the feedback resistor from Vout to FB is chosen for increased stability throughout the voltage range.

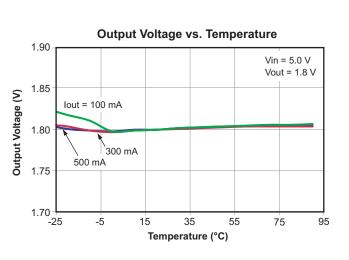
Table 1. Output Voltage Resistor Selection Table for	
Various Vout Voltages	

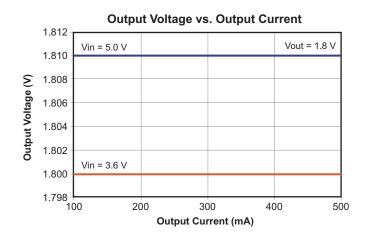
Vout (V)	R1 (kΩ)	R2 (kΩ)	L (μΗ)	Cin (μF)	Cout (μF)	C5 (pF)
0.6	0	100	1.0	10	10	100
1.1	83	100	1.0	10	10	100
1.2	100	100	1.0	10	10	100
1.3	117	100	1.0	10	10	100
1.5	150	100	1.0	10	10	100
1.6	167	100	1.0	10	10	100
1.7	183	100	1.0	10	10	100
1.8	200	100	1.0	10	10	100
1.875	213	100	1.0	10	10	100
2.5	317	100	1.0	10	10	100
2.8	367	100	1.0	10	10	100
3.3	450	100	1.0	10	10	100

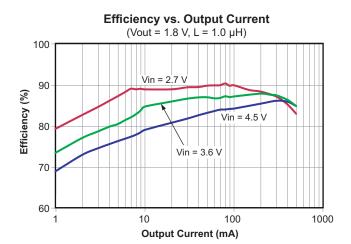


Typical Performance Characteristics

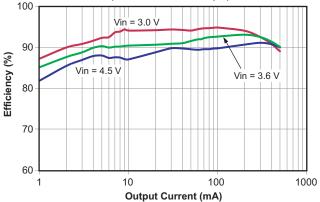


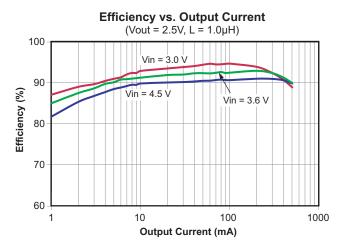






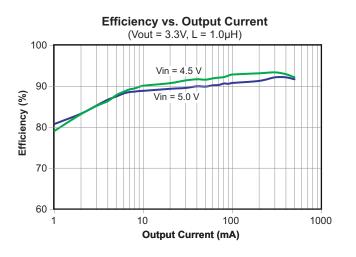
Efficiency vs. Output Current (Vout = 1.5 V, L = 1.0 μH)

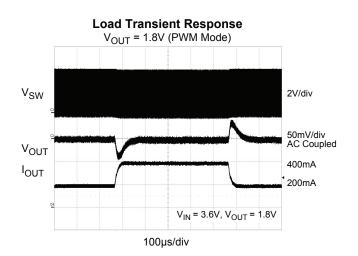


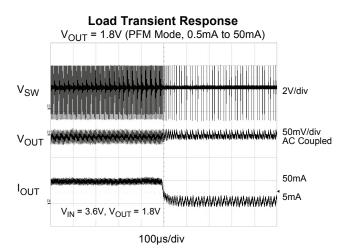


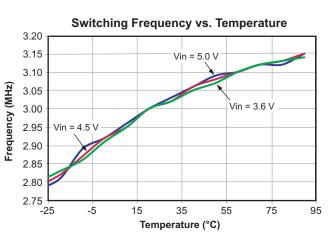
ALPHA & OMEGA SEMICONDUCTOR

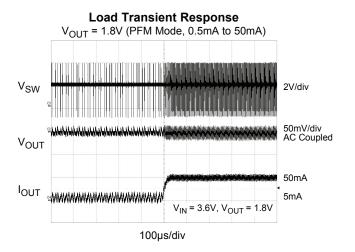
Typical Performance Characteristics (Continued)

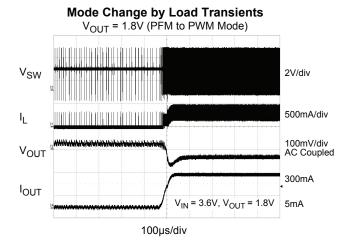






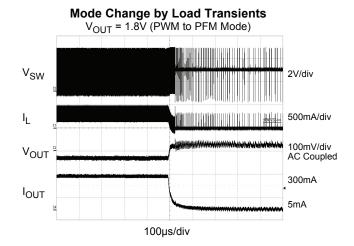


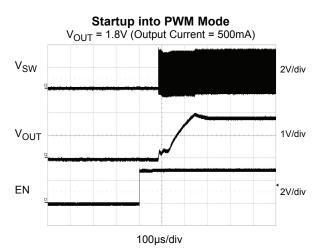


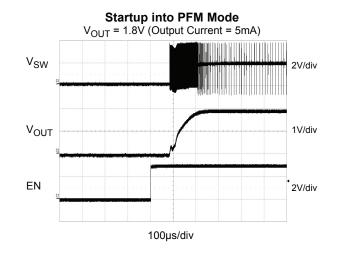


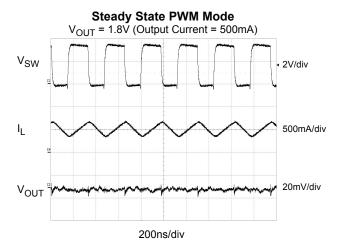


Typical Performance Characteristics (Continued)





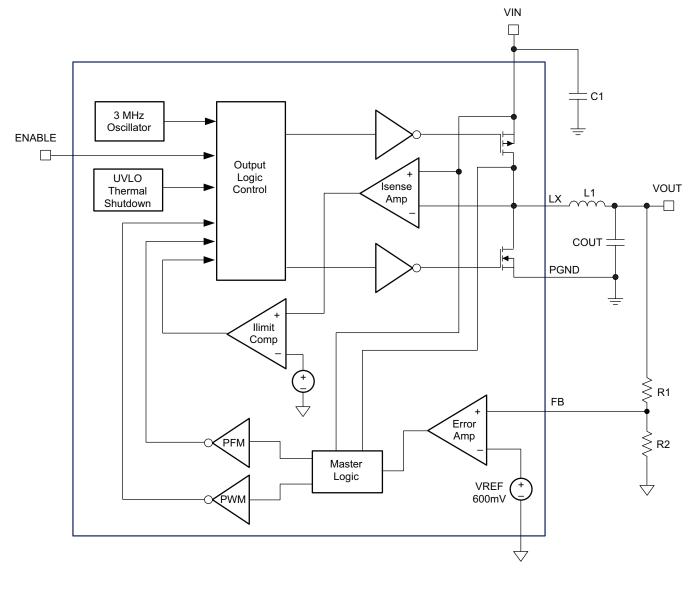






AOZ1605

Block Diagram



Operation

The AOZ1605 has a patented light load mode architecture allowing up to 85% efficiency at 1 mA load currents, enabling longer standby times in battery operated systems.

The AOZ1605 is a high efficiency step down DC-DC buck converter that operates typically at 3 MHz fixed Pulse Width Modulation (PWM) at medium to heavy load currents. The AOZ1605 can deliver a constant voltage from a single Li-Ion battery with an input voltage rail from 2.5 Volts to 5.5 Volts. Using a voltage mode architecture with synchronous rectification, the AOZ1605 has the ability to deliver up 500 mA of continuous current depending on the input voltage, output voltage, ambient temperature and inductor chosen.

There are two modes of operations depending on the current consumption, PFM (Pulse Frequency Modulation) and PWM (Pulse Width Modulation). For ultra-low current the device operates in the PFM mode to obtain high efficiency that is characteristic of the PFM mode. The device operates in the PWM mode when the output current exceed the load current of approximately 100 mA or higher.

Additional feature include under voltage lockout, over current protection, thermal shutdown and soft-start.



Inductor Selection

There are two main considerations when choosing an inductor; the inductor should not saturate, and the inductor current ripple should be small enough to achieve the desire output voltage ripple. A 1 μ H inductor with a saturation current of at least 1 A is recommended for the AOZ1605 full load application. For maximum efficiency, the inductor's resistance (DCR) should be as low as possible. For given input and output voltage, inductance and switching frequency together decide the inductor ripple current, which is,

$$\Delta I_L = \frac{V_O}{f \times L} \times \left(1 - \frac{V_O}{V_{IN}}\right)$$

The peak inductor current is:

$$I_{Lpeak} = I_0 + \frac{\Delta I_L}{2}$$

High inductance gives low inductor ripple current but requires larger size inductor to avoid saturation. Low ripple current reduces inductor core losses. It also reduces RMS current through inductor and switches, which results in less conduction loss. Usually, peak to peak ripple current on inductor is designed to be 20% to 30% of output current.

When selecting the inductor, make sure it is able to handle the peak current without saturation even at the highest operating temperature.

The inductor takes the highest current in a buck circuit. The conduction loss on inductor need to be checked for thermal and efficiency requirements.

Surface mount inductors in different shape and styles are available from Coilcraft, Elytone and Murata. Shielded inductors are small and radiate less EMI noise. But they cost more than unshielded inductors. The choice depends on EMI requirement, price and size.

Input Capacitor

The input capacitor must be connected to the V_{IN} pin and PGND pin of AOZ1605 to maintain steady input voltage and filter out the pulsing input current. The voltage rating of input capacitor must be greater than maximum input voltage plus ripple voltage. For greater capacitor performance, the working capacitance voltage should be twice Vin.

The input ripple voltage can be approximated by equation below:

$$\Delta V_{IN} = \frac{I_O}{f \times C_{IN}} \times \left(1 - \frac{V_O}{V_{IN}}\right) \times \frac{V_O}{V_{IN}}$$

Since the input current is discontinuous in a buck converter, the current stress on the input capacitor is another concern when selecting the capacitor. For a buck circuit, the RMS value of input capacitor current can be calculated by:

$$I_{CIN_RMS} = I_{O} \times \sqrt{\frac{V_{O}}{V_{IN}}} \left(1 - \frac{V_{O}}{V_{IN}}\right)$$

if we let *m* equal the conversion ratio:

$$\frac{V_0}{V_{IN}} = m$$

The relationship between the input capacitor RMS current and voltage conversion ratio is calculated and shown in Figure 1 below. It can be seen that when V_O is half of V_{IN} , C_{IN} is under the worst current stress. The worst current stress on C_{IN} is 0.5 x I_O .

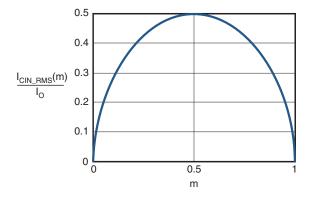


Figure 3. I_{CIN} vs. Voltage Conversion Ratio

For reliable operation and best performance, the input capacitors must have current rating higher than I_{CIN_RMS} at worst operating conditions. Ceramic capacitors are preferred for input capacitors because of their low ESR and high current rating. When selecting ceramic capacitors, X5R or X7R type dielectric ceramic capacitors should be used for their better temperature and voltage characteristics. Note that the ripple current rating from capacitor manufactures are based on certain amount of life time. Further de-rating may be necessary in practical design.



Output Capacitor

The output capacitor is selected based on the DC output voltage rating, output ripple voltage specification and ripple current rating.

The selected output capacitor must have a higher rated voltage specification than the maximum desired output voltage including ripple. De-rating needs to be considered for long term reliability.

Output ripple voltage specification is another important factor for selecting the output capacitor. In a buck converter circuit, output ripple voltage is determined by inductor value, switching frequency, output capacitor value and ESR. It can be calculated by the equation below:

$$\Delta V_{O} = \Delta I_{L} \times \left(ESR_{CO} + \frac{1}{8 \times f \times C_{O}} \right)$$

where,

C_O is output capacitor value and

ESR_{CO} is the Equivalent Series Resistor of output capacitor.

When low ESR ceramic capacitor is used as output capacitor, the impedance of the capacitor at the switching frequency dominates. Output ripple is mainly caused by capacitor value and inductor ripple current. The output ripple voltage calculation can be simplified to:

$$\Delta V_{O} = \Delta I_{L} \times \frac{1}{8 \times f \times C_{O}}$$

If the impedance of ESR at switching frequency dominates, the output ripple voltage is mainly decided by capacitor ESR and inductor ripple current. The output ripple voltage calculation can be further simplified to:

$$\Delta V_{O} = \Delta I_{L} \times ESR_{CO}$$

For lower output ripple voltage across the entire operating temperature range, X5R or X7R dielectric type of ceramic, or other low ESR tantalum are recommended to be used as output capacitors.

In a buck converter, output capacitor current is continuous. The RMS current of output capacitor is decided by the peak to peak inductor ripple current. It can be calculated by:

$$I_{CO_RMS} = \frac{\Delta I_L}{\sqrt{12}}$$

Usually, the ripple current rating of the output capacitor is a smaller issue because of the low current stress. When the buck inductor is selected to be very small and inductor ripple current is high, output capacitor could be overstressed.

Thermal Shutdown

In most applications the AOZ1605 does not dissipate much heat due to its high efficiency. But in an application where the AOZ1605 is running at high ambient temperature with low supply voltage and high duty cycle, the heat dissipated may exceed the maximum junction temperature. If the junction temperature reaches approximately 140 °C (typical), the internal High Side and Low Side MOSFET switching is disabled until the temperature on the die has sufficiently fallen below 105°C. The device remains in thermal shutdown until the junction temperature falls below the thermal shutdown hysteresis.

Undervoltage Lockout

The undervoltage lockout circuit prevents the device from malfunctioning at low input voltages and from excessive discharge of the battery by disabling the output stage of the converter. The AOZ1605 will resume normal operation when the input supply voltage rises high enough to properly function. The undervoltage lockout threshold is typically 2.3 Volts.

Soft Start

The AOZ1605 has a soft-start circuit that limits the inrush current during startup. Soft start is activated when EN goes from logic low to logic high after Vin reaches 2.3 Volts.

Over Current Protection (OCP)

The sensed inductor current signal is also used for over current protection. Since the AOZ1605 employs peak current mode control, the COMP pin voltage is proportional to the peak inductor current. The COMP pin voltage is limited to be between 0.4 V and 2.5 V internally. The peak inductor current is automatically limited cycle by cycle.

When the output is shorted to ground under fault conditions, the inductor current decays very slow during a switching cycle because of $V_0 = 0$ V. To prevent catastrophic failure, a secondary current limit is designed inside the AOZ1605. The measured inductor current is compared against a preset voltage which represents the current limit, approximately 1 A. When the output current is more than current limit, the high side switch will be turned off. The converter will initiate a soft start once the over-current condition disappears.



Enable

The EN pin of the AOZ1605 is active high. Connect the EN pin to VIN if enable function is not used. Pull it to ground will disable the AOZ1605. Do not leave it open. The voltage on EN pin must be above 2 V to enable the AOZ1605. When voltage on EN pin falls below 0.6 V, the AOZ1605 is disabled. If an application circuit requires the AOZ1605 to be disabled, an open drain or open collector circuit should be used to interface to EN pin.

Low Drop Out Operation

The AOZ1605 can operate at 100% duty cycle. In this state, the high side p-channel MOSFET is always on. This will allow the output to follow the input voltage as it drops below the regulation voltage.

Thermal Management and Layout Considerations

In the AOZ1605 buck regulator circuit, high pulsing current flows through two circuit loops. The first loop starts from the input capacitors, to the VIN pin, to the LX pin, to the filter inductor, to the output capacitor and load, and then return to the input capacitor through ground. Current flows in the first loop when the high side switch is on. The second loop starts from inductor, to the output capacitors and load, to the low side NMOSFET. Current flows in the second loop when the low side NMOSFET is on.

In PCB layout, minimizing the two loops area reduces the noise of this circuit and improves efficiency. A ground plane is strongly recommended to connect input capacitor, output capacitor, and PGND pin of the AOZ1605.

In the AOZ1605 buck regulator circuit, the major power dissipating components are the AOZ1605 and the output inductor. The total power dissipation of converter circuit can be measured by input power minus output power.

$$P_{total_loss} = V_{IN} \times I_{IN} - V_O \times I_O$$

The power dissipation of inductor can be approximately calculated by output current and DCR of inductor.

$$P_{inductor_loss} = I_0^2 \times R_{inductor} \times 1.1$$

The actual junction temperature can be calculated with power dissipation in the AOZ1605 and thermal impedance from junction to ambient.

$$T_{junction} = (P_{total_loss} - P_{inductor_loss}) \times \Theta_{JA}$$

The maximum junction temperature of AOZ1605 is 140 °C, which limits the maximum load current capability. Please see the thermal de-rating curves for maximum load current of the AOZ1605 under different ambient temperature.

The thermal performance of the AOZ1605 is strongly affected by the PCB layout. Extra care should be taken by users during design process to ensure that the IC will operate under the recommended environmental conditions.



The AOZ1605 is an exposed pad DFN-8 package. Several layout tips are listed below for the best electric and thermal performance.

- 1. The exposed pad is connected to PGND. Connect a large copper plane to this pad to help thermal dissipation.
- 2. Do not use thermal relief connection from the VIN pin and the PGND pin. Pour a maximized copper area to the PGND pin and the VIN pin to help thermal dissipation.
- Input capacitor should be connected as close as possible to the VIN pin and the PGND pin. For optimal performance of the device, place bulk capacitor and de-coupling capacitor no further than 50 mils from the device.

- 4. A ground plane is preferred. If a ground plane is not used, separate PGND from AGND and connect them only at one point to avoid the PGND pin noise coupling to the AGND pin.
- 5. Make the current trace from LX pin to L to Co to PGND as short as possible.
- Pour copper planes on all unused board area and connect them to stable DC nodes, like VIN, GND or VOUT.
- 7. Keep sensitive signal traces away from the LX pin.

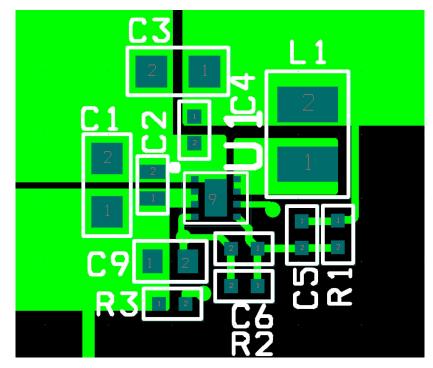
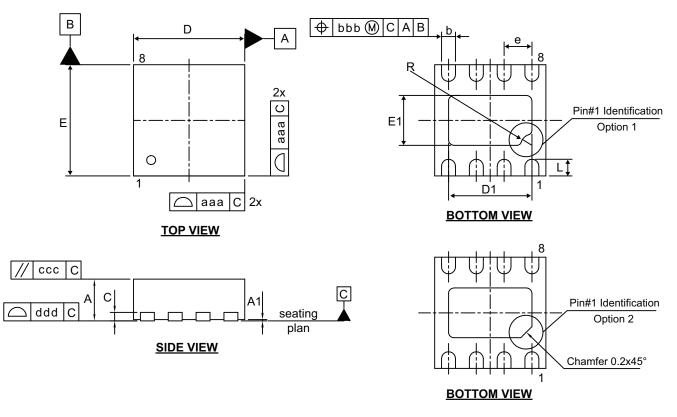
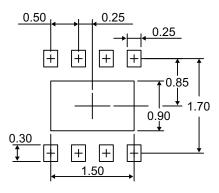


Figure 2. AOZ1605 (DFN-8) PCB Layout

Package Dimensions, DFN 2x2, 8L



RECOMMENDED LAND PATTERN





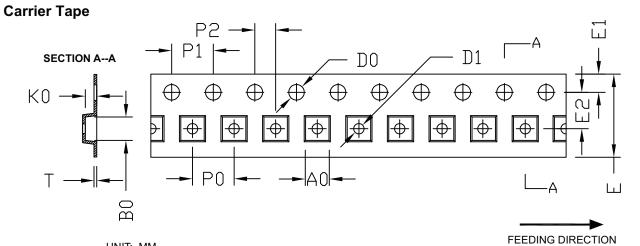
Dimensions in millimeters Dimensions in inches Symbols Symbols Min. Nom. Max. Min. Nom. Max. A 0.70 0.75 0.80 А 0.028 0.030 0.031 A1 0.00 0.02 0.05 A1 0.000 0.001 0.002 b 0.18 0.25 0.30 b 0.007 0.010 0.012 0.20 REF 0.008 REF С С 2.00 0.075 0.079 D 1.90 2.10 D 0.083 D1 1.35 1.50 1.60 D1 0.053 0.059 0.063 Е Е 0.075 0.079 0.083 1.90 2.00 2.10 0.75 0.90 0.030 0.035 0.039 E1 1.00 E1 е 0.50 BSC е 0.020 BSC 0.20 800.0 0.012 0.30 0.40 L 0.016 L R R 0.008 0.20 aaa 0.15 aaa 0.006 0.004 bbb 0.10 bbb 0.10 0.004 ссс ccc ddd 0.08 ddd 0.003

Notes:

- 1. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
- 2. Controlling dimension is in millimeter, converted inch dimensions are not necessarily exact.
- 3. Dimension **b** applies to matellized terminal and is measured between 0.10mm and 0.30mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension **b** should not be measured in that radius area.
- 4. Coplanarity ddd applies to the terminals and all other bottom surface metallization.

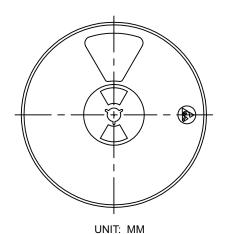


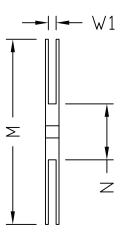
Tape and Reel Dimensions, DFN 2x2, 8L

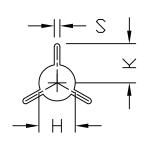


UNIT: MM **B0** K0 D0 D1 Е E1 E2 **P0 P1 P2** т Package A0 2.25 2.25 1.00 1.50 1.00 8.00 1.75 3.50 4.00 4.00 2.00 0.254 DFN 2x2 ±0.05 ±0.10 ±0.25 ±0.30 ±0.10 ±0.05 ±0.10 ±0.05 ±0.02 ±0.05 ±0.05 ±0.10 -0.10

Reel

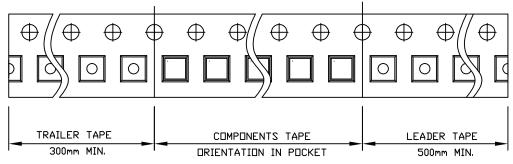






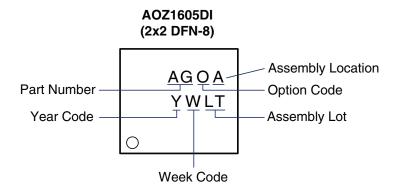
Tape Size	Reel Size	м	Ν	W1	W2	Н	S	К
8mm	Ø177.8	Ø177.8 MAX.	53.6 MIN.	8.4 +2.5 -0.0	14.4 MAX.	13.0 +0.5 -0.3	1.5 MIN.	10.1 MIN.

Leader/Trailer and Orientation





Part Marking



This datasheet contains preliminary data; supplementary data may be published at a later date. Alpha & Omega Semiconductor reserves the right to make changes at any time without notice.

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